In the Claims:

1. - 23. Cancelled

24. (Currently Amended) A method of forming a semiconductor ~~devise,~~ device, the method comprising:

forming a cell gate oxide in a cell region;

forming a logic gate oxide in a periphery region;

forming a first doped polysilicon layer on the cell gate oxide; and

forming a second polysilicon layer, the second polysilicon layer being [[on]] in contact with the logic gate oxide in the periphery region and [[on]] in contact with the first doped polysilicon layer in the cell region.

25. (Original) The method of claim 24 wherein the second polysilicon layer positioned above the cell gate oxide is a p-type doped polysilicon.

26. (Original) The method of claim 25 wherein the second polysilicon layer is doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

27. (Currently Amended) The method of claim 24 wherein the step of forming a first doped polysilicon layer is performed by depositing by furnace an in-situ doped polysilicon.

28. (Original) The method of claim 27 wherein depositing by furnace is performed at a temperature of about 540° C to about 640° C.

29. (Original) The method of claim 24 wherein the second polysilicon layer is formed of undoped polysilicon.

30. (Original) The method of claim 24 further comprising the step of doping the second polysilicon layer located above the cell gate oxide with a p-type dopant.

31. (Original) The method of claim 30 further comprising the step of doping the second polysilicon layer located above the logic gate oxide with an n-type dopant.

32. (Original) The method of claim 30 further comprising the step of doping the second polysilicon layer located above the logic gate oxide with a p-type dopant.

33. (Original) The method of claim 30 wherein the p-type dopant is selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.